

## CLAIMS

What is claimed is:

- 1 1. A fault-tolerant data processing apparatus comprising:
- 2 a plurality of data processing elements executing substantially identical instruction
- 3 streams substantially simultaneously;
- 4 a target in communication with at least one of the plurality of data processing
- 5 elements; and
- 6 a switching fabric communicating transactions asynchronously between at least
- 7 one of the plurality of data processing elements and the target.
- 1 2. The apparatus of claim 1 wherein the plurality of data processing elements
- 2 execute the same instruction in lock-step synchronization.
- 1 3. The apparatus of claim 1 wherein each of the plurality of data processing elements
- 2 comprises a Central Processing Unit (CPU).
- 1 4. The apparatus of claim 3 wherein the CPU further comprises a plurality of
- 2 processors.
- 1 5. The apparatus of claim 1 wherein the target is a data processing element.
- 1 6. The apparatus of claim 1 wherein the target is a peripheral component.
- 1 7. The apparatus of claim 6 wherein a channel adapter interconnects the peripheral
- 2 component to the switching fabric.
- 1 8. The apparatus of claim 1 wherein a plurality of channel adapters interconnect,
- 2 respectively, each of the plurality of data processing elements to the switching fabric.

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1 9. The apparatus of claim 1 further comprising a plurality of voter delay buffers  
2 wherein each of the plurality of voter delay buffers is in communication with at least one  
3 of the plurality of data processing elements.

1 10. The apparatus of claim 1 further comprising a plurality of direct memory access  
2 (DMA) engines in communication with the switching fabric.

1 11. The apparatus of claim 1 wherein the plurality of data processing elements are  
2 identified by a node address.

1 12. The apparatus of claim 1 wherein each of the plurality of data processing elements  
2 is individually identified by a respective device address.

1 13. The apparatus of claim 1 wherein the transaction comprises at least one  
2 information packet.

1 14. A method for fault tolerant digital data processing comprising:

2 (a) generating by a plurality of data processing elements identical transactions  
3 each having a target address; and

4 (b) communicating the identical transactions asynchronously on a switching  
5 fabric to the target identified by the target address.

1 15. The method of claim 14 wherein step (b) comprises:

2 (b-a) communicating identical transactions to a voting unit; and

3 (b-b) transmitting by the voting unit a single transaction asynchronously on a  
4 switching fabric.

1 16. The method of claim 14 wherein the target address is a node address.

1 17. The method of claim 14 wherein the target address is a device address.

1 18. The method of claim 14 wherein the target of step (b) is a peripheral component.

1 19. The method of claim 14 wherein step (b) further comprises:

2 (b-a) communicating each of the identical transactions from each of the plurality  
3 of data processing elements to each of a plurality of channel adapters;

4 (b-b) communicating each of the identical transactions from each of the plurality  
5 of channel adapters to the switching fabric;

6 (b-c) communicating the identical transaction from the switching fabric to a  
7 channel adapter; and

8 (b-d) communicating the identical transaction from the channel adapter to the target.

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